

REMARKS

Prior to the present amendment, the present application contained Claims 1-7. Claims 1 and 5 have been amended. Accordingly, following the entry of this Reply, Claims 1-7 will be at issue in the present application. Reconsideration of the present application is respectfully requested in view of the above amendments and following remarks.

Enclosed herewith is a replacement drawing sheet containing amendments to drawing Figures 6A and 6B. These amendments correct typographical errors, wherein the word "flame" has been changed to --frame--. Also enclosed herewith is an Annotated Drawing Sheet, indicating the amendments to Figs. 6A and 6B in red. Approval of the amended drawings is requested.

Claims 1-4 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,531,284 to Watanabe et al. (hereinafter "Watanabe"). Applicants submit that Watanabe does not teach all of the limitations of the claims.

As illustrated in Fig. 5 of the present application, and described in the specification at page 11, lines 7-20 and page 12, lines 2-18, the frame transfer type solid state image sensor first keeps the transfer electrodes deactivated ($\phi v1-\phi v4$). The transfer electrodes are then activated to store new information charges. As illustrated in Fig. 5, the vertical clock signals $\phi v1-\phi v4$ are dropped after frame transfer is completed. In this state, the substrate clock signal ϕb is in low level. In response to a shutter trigger, ST, the substrate clock signal ϕb rises but the vertical clock signals $\phi v1-\phi v4$ are kept at low level. Advantages of the present invention are described from page 12, line 28 through page 14, line 2. That is, substantially all of the unnecessary information charges residing in the channel region are discharged even if the shutter operation is fast. This prevents unnecessary information charges from residing in the channel region. Since the amount of charges discharged during the shutter operation is small, the charges are discharged sufficiently even if the potential of the substrate clock b is low.

Watanabe discloses a timing chart of a substrate clock signal ϕb and a vertical clock signal ϕv in Fig. 2. After frame transfer is completed, the vertical clock signal ϕv is not dropped. When the substrate clock signal ϕb rises, the vertical clock signal ϕv also rises. Accordingly, there is no teaching or suggestion in Watanabe of keeping the plurality of transfer electrodes deactivated prior to rising substrate potential. Therefore, Applicants submit that Claim 1, as amended, is allowable

over Watanabe. Furthermore, Applicants submit that claims 2-4, which depend (directly or indirectly) from claim 1 are also allowable for at least the same reasons as described with respect to claim 1.

Claims 5-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe and Japanese Publication No. 09-168118 (Yadokoro et al.).

It is respectfully submitted that Claim 5, as amended, is allowable over the cited references for similar reasons as described above in connection with the Watanabe reference. More specifically, Applicants submit that none of the cited references, alone or in combination, teach or suggest keeping the plurality of transfer electrodes deactivated prior to rising substrate potential. Watanabe and Yadokoro fail to disclose at least this feature of the invention as claimed in Claim 5. Accordingly, Applicants submit that Claim 5 is allowable over the cited references. Furthermore, Applicants submit that Claims 6-7, which depend (directly or indirectly) from Claim 5 are also allowable for at least the same reasons as Claim 5.

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,
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